

A novel single-phase PWM asymmetrical multilevel inverter with number of semiconductor switches reduction

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ABSTRACT

In this paper, a new asymmetrical multilevel inverter topology (MLI) is proposed with the objectives of using decreased number of semiconductor switches, dc voltage sources, gate driver circuits and dc links. The structure of presented MLI is very simple and modular. The fundamental module of this structure consists of nine semiconductor switches (eight unidirectional and one bidirectional) and four asymmetrical configured DC sources (ratio of 1:2), which can generate 13-level output voltage. To validate the design, a Matlab-Simulink based model is developed. For this paper, a Sinusoidal Pulse Width Modulation (SPWM) is deployed as the switching strategy of the proposed MLI. The circuit model is simulated under pure resistive and inductive loads. It will be shown that the circuit performs well under both loads. Comparison with traditional MLIs and other recently introduced MLIs will be conducted to show the superiority of the proposed MLI in terms of reduced number of devices and lower voltage stress across the switches.

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1. INTRODUCTION

Multilevel inverters (MLI) are gaining more attention in industry and academia due to their performance superiority over traditional two-level inverter in terms of high power quality, lower voltage/current harmonics, and lower voltage stresses on switches. The MLI are used in various applications such as renewable energy sources [1-3], distributed generations and high voltage direct current [4, 5], electrical motor drives [6, 7], active power filters [8], electrical vehicle, micro-grid [9], distribution static compensator [10] and flexible alternating current transmission devices [11, 12].

The traditional MLI circuit are the cascaded H-bridge MLI, neutral-point clamped [13] and flying-capacitor clamped MLI [14]. Among them, the cascaded H-bridge MLI receives wider attention in practice due to its simplicity of control and modularity in structure. The idea of MLI circuit was first introduced by Baker and Bannister [15] in 1970s by describing a converter topology that is able to produce staged-output voltage that resembles a sinusoidal waveform by connecting several H-bridge inverters in cascaded fashion. The neutral-point clamp was presented by Baker in 1980. This topology uses clamping diodes to clamp the switch voltage from a single dc source [13]. The flying-capacitor MLI [14] was proposed by T. Meynard in 1992. The topology has identical structure with the former topology but uses clamping capacitors instead of clamping diodes.

For MLI, higher number of output voltage level generation is desirable to improve the harmonics profile of the output voltage. Moreover, it can reduce the size of the output filter. However, it was known that MLI requires more components if extended for higher voltage levels production. This can lead to overall system to be costly, bulky and reliability is reduced. To overcome this limitation, research on reduced device

count MLI topologies are gaining momentum. Several promising topologies have been introduced in recent years [16-21]. Generally, the MLI topologies can be categorized under two groups, namely the symmetrical topologies, where all dc sources are have equal magnitudes and asymmetrical topologies, where dc voltage sources have distinct voltage ratios. The former type of topology is preferred since it can produce higher number of output voltage level using the same amount of devices. Several number of asymmetrical MLI topologies have been proposed in [22-27]. In [28] new multilevel inverter topology known as packed U-cell (PUC) is presented. This topology consists of packed U-cell where each cell is comprised of two semiconductor devices and a dc voltage source.

In this paper, a new multilevel inverter with the objective to reduce the number of components count is proposed. It uses a nine switches and four assymetric dc sources to generate 13-level of output voltage. The proposed topology model will be developed via Matlab-Simulink software and simulate under different type of load to validate its viability. The sinusoidal pulse width modulation (SPWM) strategy will be deployed as the switching strategy for the proposed MLI. From the result, the proposed MLI performs well under inductive load.

2. PROPOSED TOPOLOGY

In this paper, a new MLI with reduced device count is proposed. Fundamental unit of the proposed MLI topology is shown in Figure 1. It comprises of eight unidirectional S_1 to S_8 , one bidirectional switch S_9 and four voltage sources. The unidirectional switches consist of an IGBT and an antiparallel diode. The bidirectional switch consists of two IGBTs, two diodes and a gate driver circuit. An anti-parallel diode is used to conduct current in both directions and block voltage in one direction.

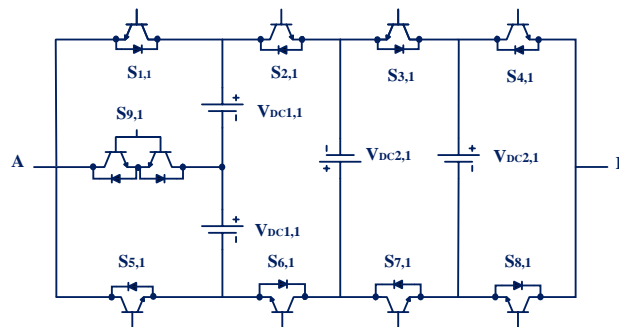


Figure.1 Fundamental block of the proposed MLI topology

Table 1. Switching states for 13-level MLI

States		Switch states									V_0
		S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	
Positive levels	1	0	0	0	0	0	1	1	1	1	1V
	2	1	0	0	0	0	1	1	1	0	2V
	3	0	0	1	1	0	1	0	0	1	3V
	4	1	0	1	1	0	1	0	0	0	4V
	5	0	0	1	0	0	1	0	1	1	5V
Zero level	6	1	0	1	0	0	1	0	1	0	6V
	7	1	1	1	1	0	0	0	0	0	0V
	8	0	1	1	1	0	0	0	0	1	-1V
Negative levels	9	0	1	1	1	1	0	0	0	0	-2V
	10	0	1	0	0	0	0	1	1	1	-3V
	11	0	1	0	0	1	0	1	1	0	-4V
	12	0	1	0	1	0	0	1	0	1	-5V
	13	0	1	0	1	1	0	1	0	0	-6V

Magnitude of the two DC input voltage sources is V_1 each and the other two sources has magnitude of V_2 each as shown in (1) and (2). The fundamental unit is capable to produce thirteen voltage levels in the output. To avoid short-circuit of dc voltage inputs, simultaneous conduction of switch pairs (S_1 , S_9) (S_5 , S_9) (S_2 , S_6) (S_3 , S_7) and (S_4 , S_8) should be avoided. Switching states to produce 13-level output voltage are shown in Table 1.

$$V_1 = 1V_{DC}; \quad (1)$$

$$V_2 = 2V_{DC}; \quad (2)$$

This voltage source configuration can produce thirteen voltage levels of $0V, \pm 1V_{DC}, \pm 2V_{DC}, \pm 3V_{DC}, \pm 4V_{DC}, \pm 5V_{DC}$ and $\pm 6V_{DC}$ in the output.

2.1. Total voltage stress

One of important parameter in evaluating the performance of the MLI topologies is the total voltage stress (TVS) of topology. It is desirable to obtain low TVS since it also reflects the development cost of the topology. Higher TVS, meaning that one need to use switch that has high blocking voltage capability, which normally expensive to procure [22]. The blocking voltage of the semiconductor switch is the total voltage stress to withstand in its off-state. The maximum blocking voltage by each switch in proposed topology can be obtained through (3)-(7).

$$V_{S1} = V_{S5} = 1V_{DC} + 1V_{DC} = 2V_{DC}; \quad (3)$$

$$V_{S3} = V_{S7} = 2V_{DC} + 2V_{DC} = 4V_{DC}; \quad (4)$$

$$V_{S9} = 2V_{DC}; \quad (5)$$

$$V_{S4} = V_{S8} = 2V_{DC} + 2V_{DC} = 4V_{DC}; \quad (6)$$

$$V_{S2} = V_{S6} = 1V_{DC} + 1V_{DC} + 2V_{DC} = 4V_{DC}; \quad (7)$$

Therefore, Total voltage stress (TVS) of all the semiconductor switches utilized in fundamental block can be calculated by adding all the blocked voltages as shown in (8).

$$\begin{aligned} \text{TVS} &= V_{S1} + V_{S2} + V_{S3} + V_{S4} + V_{S5} + V_{S6} \\ &+ V_{S7} + V_{S8} + V_{S9} = 2V_{DC} + 4V_{DC} + 4V_{DC} + 2V_{DC} + 2V_{DC} + 4V_{DC} + 4V_{DC} + 2V_{DC} + 2V_{DC} \\ \text{TVS} &= 26V_{DC}; \end{aligned} \quad (8)$$

2.2. Extention to n-level output voltage

Fundamental unit of the proposed topology can be easily cascaded to generate higher number of output voltage levels. Figure 2 depicts the generalized circuit of the presented topology for n-level output. The cascaded structure is able of produce higher number of level with suitable DC source selection. The number of levels of the output voltage waveform for n blocks structure can be determined using equation (9). Term (10) and (11), represent the maximum output voltage for n units and the total number of IGBTs required, respectively.

$$N_L = 12n + 1; \quad (9)$$

$$V_{o,max} = V_{o,1} + V_{o,2} + V_{o,3} + \dots + V_{o,n}; \quad (10)$$

$$N_{IGBT} = 5(N_L - 1)/6; \quad (11)$$

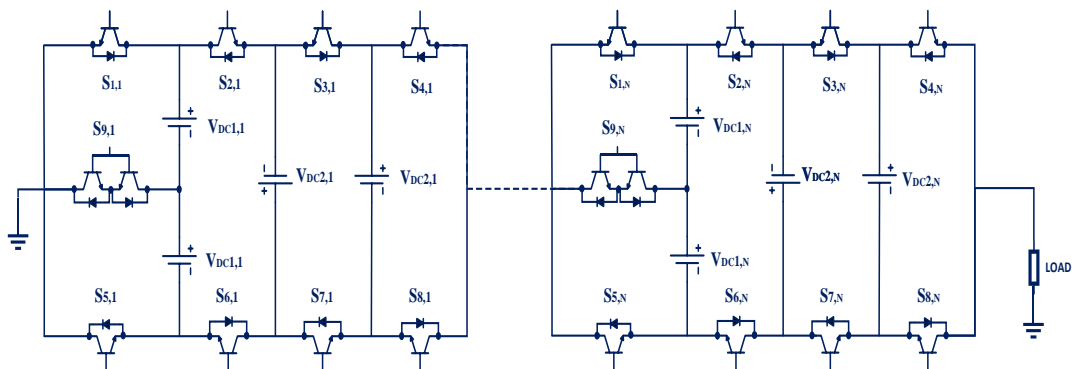


Figure 2. Generalized structure of MLI topology

3. COMPARISON WITH OTHER TOPOLOGIES

Comparison with the traditional and recent reduced components MLI topologies is conducted to validate the effectiveness of the proposed MLI. Table 2 summarised the comparison for several MLI topologies for 13-level output voltage. In terms of IGBT counts, it is confirmed that the proposed MLI structure has the least number of IGBT counts. The proposed MLI has the lowest number of TVS as compared to other recent MLI topologies except when comparing with MLI of [16]. However, it should be noted that the MLI proposed in [16] employs H-bridge for polarity reversal. The voltage stress across the switches of the H-bridge are equals to its MLI's output voltage, hence may limit its usage to medium power applications only. As for traditional MLIs, all of them yield TVS of 24, which is lower than the proposed MLI, which is 26. However, the proposed MLI is still considered as a good alternative to the traditional MLIs due to low IGBT counts. The proposed MLI multilevel inverter has higher amount of variety of dc input voltage sources (N_{variety}) compared to other mentioned topologies. Higher variety of dc source means that the proposed MLI can be configured as symmetrical or asymmetrical MLI.

Table 2. Comparison with other 13-level inverter topologies

Type	IGBTs	Drivers	N_{variety}	Diodes	Dc links	$\text{TVS} \times V_{\text{DC}}$	Negative levels
CHB	24	24	1	24	6	24	With H-bridge
FC	24	24	1	24	6	24	Inherent
NFC	24	24	1	24	6	24	inherent
MLDCL	16	16	1	16	6	36	With H-bridge
ST-Type	12	9	2	12	4	30	inherent
[16]	14	14	2	14	6	24	With H-bridge
proposed	10	9	2	10	4	26	inherent

4. DESIGN OF SIMULATION MODEL

To validate the performance of proposed MLI topology, simulations are performed using computer software tool Matlab/Simulink. Simulation model of the proposed fundamental unit is illustrated in Figure 3. The value of the DC sources are configured in the ratio of 1:2. The value for $V_{\text{dc1,1}} = 15 \text{ V}$ while $V_{\text{dc1,2}} = 30 \text{ V}$, respectively. The simulation model will be tested under different load type. The first test will be for pure resistive load with $R = 100 \Omega$ and the second test will be an inductive load with $R = 40 \Omega$ and $L = 200 \text{ mH}$.

For switching strategy, a multi-carrier based Phase-Disposition sinusoidal pulse width modulation will be deployed for producing the gating signals. Figure 4 shows the PD-PWM waveform diagram. The frequency of the triangular carriers is depends on the switching frequency of the proposed MLI. The number of triangular carriers can be calculated as (12).

$$\text{Number of carrier} = N_L - 1 \quad (12)$$

Sinusoidal reference wave of 50 Hz is compared with all carrier waves to create pulses for switching of devices. Figure 5 shows the gate pulses of the switches S_1 to S_9 for 13-level MLI. The triangular carrier frequency is 5k Hz.

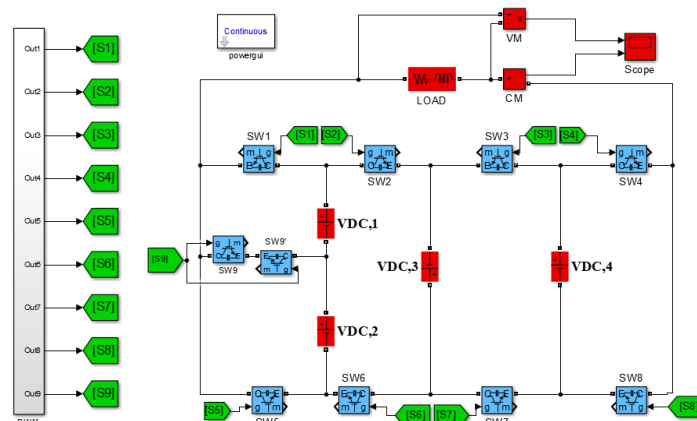


Figure 3. Simulation model of the proposed multilevel inverter for 13-level voltage generation

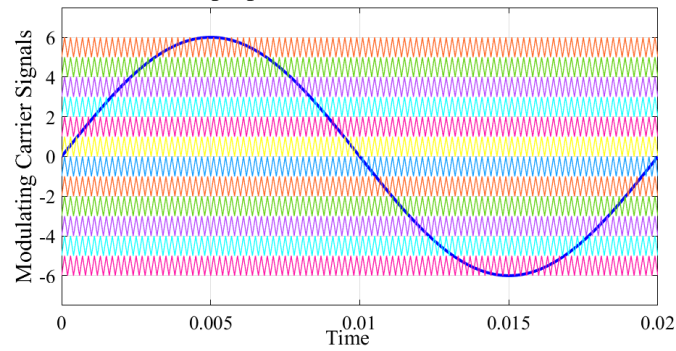


Figure 4. Phase disposition PWM waveform generation

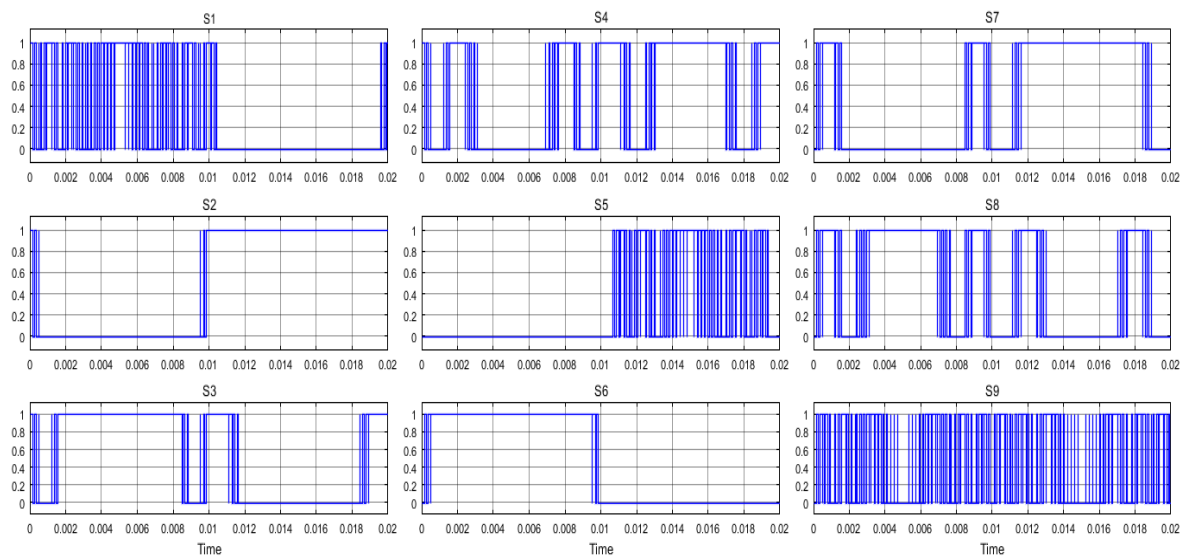
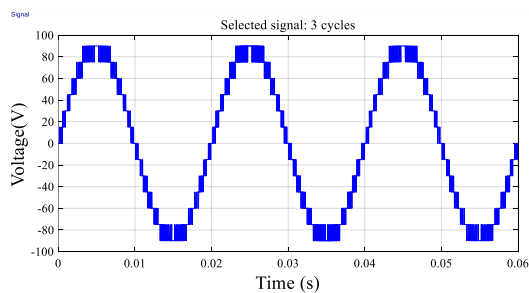
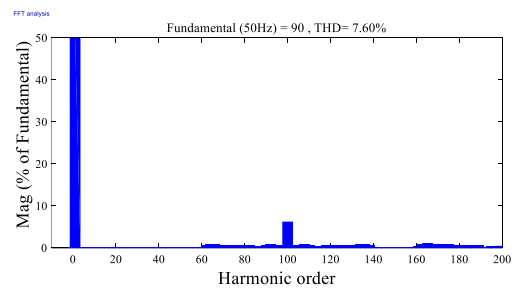


Figure 5. Switching pulses for 13-level MLI topology

Figures 6(a)–(d) exhibit the output voltage, output current and the harmonics spectrum when connected with $R=100\ \Omega$. As clearly be seen from Figure 6(a), the simulation model is able to produce output voltage of 13-level as expected. The fundamental voltage component is 90 V and the total harmonics distortion is 7.6%. Figures 7(a)–(d) exhibit the output voltage, current and the harmonics spectrum when connected with inductive load $R=40\ \Omega$ and $L=200\text{ mH}$. The total harmonics distortion for voltage and current is 7.6% and 0.38%, respectively. Frequency spectrum for output voltage confirms that the magnitude of each harmonic is less than 5% which meet IEEE519 standards (magnitude of THD is equal to or less than 8% and magnitude of each order harmonic is equal to or less than 5%).



(a)



(b)

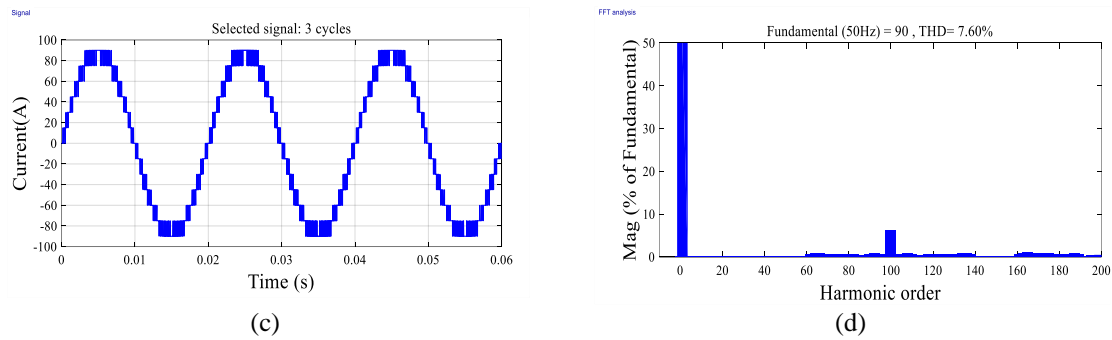


Figure 6. Simulation results of output voltage and current waveform when connected with $R = 100\Omega$, (a) Output voltage, (b) Output Voltage THD, (c) Output Current, (d) Output Current THD

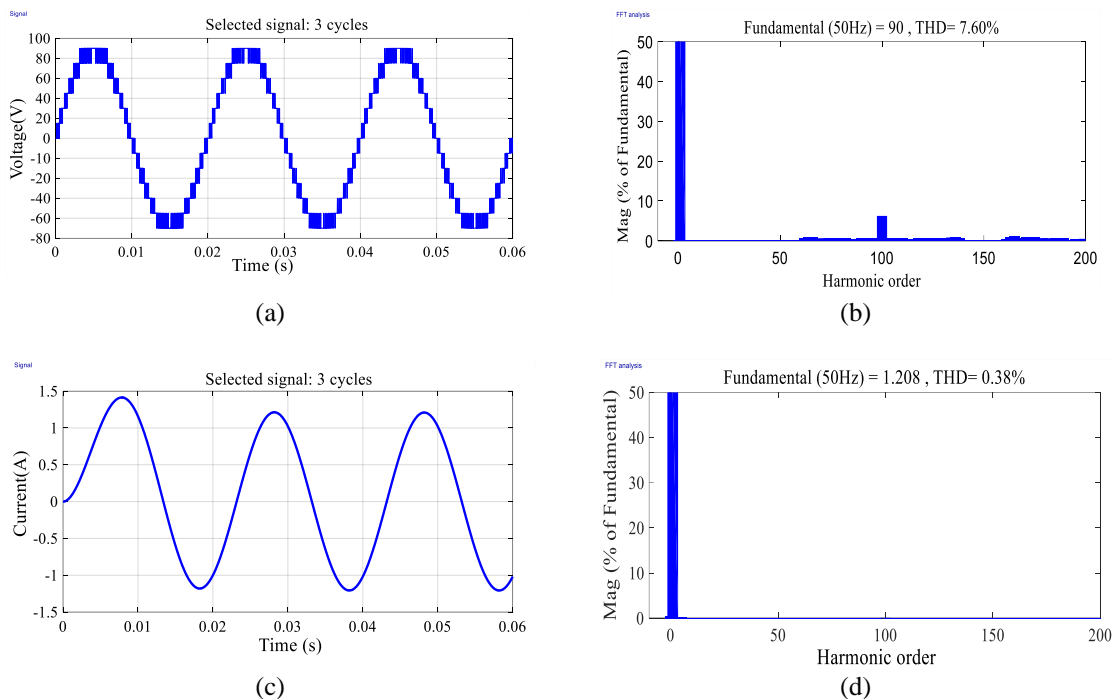


Figure 7. Simulation results for output voltage and current when connected with inductive load $R = 40\Omega$ and $L = 200\text{mH}$, (a) Output voltage, (b) Output Voltage THD, (c) Output Current, (d) Output Current THD

5. CONCLUSION

In this paper, a new multilevel inverter topology utilizing less device count is presented. It can generate 13-level output voltage using nine switches and four asymmetrical DC sources. It can be easily extended for higher number of voltage levels with less number of power devices and decreased voltage stress on semiconductor devices. The main characteristic of the presented topology is that it has the capability to produce all voltage levels without need of H-bridge circuit. A Phase-Disposition PWM switching strategy is employed to generate switching signals for the proposed MLI topology. From the simulation results, it was found that the proposed topology is able to generate 13-level output voltage with low total harmonics distortion.

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